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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/164,123	09/30/98	MAYER A	GR-97-P-2681

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EXAMINER	
EATON,K	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 04/13/00

Pleas find below and/or attached an Office communication concerning this application or pr ceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/164,123	MAYER, ALBRECHT	
	Examiner	Art Unit	
	Kurt M Eaton	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *31 August 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *12-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☒ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

14) ☒ Notice of References Cited (PTO-892)
15) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
16) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
17) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
18) ☐ Notice of Informal Patent Application (PTO-152)
19) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group II in Paper No. 7 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 12-14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 7.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being unpatentable over Kuriyama.

In re claim 1, Kuriyama shows in Figures 1 and 2 a method for producing an electrical connection between integrated circuits, which includes: providing a first integrated circuit (7) having a terminal (12) and a signal terminal (11); forming an electrically conductive connection (10c) between the terminal and the signal terminal of the first integrated circuit; providing a second integrated circuit (3) having a terminal (3c) that is electrically coupled to a protective structure (10c) for protecting against electrostatic discharges; disposing the first and second integrated circuits adjacent one another; electrically connection the signal terminal of the first integrated circuit to the terminal of the second integrated circuit; and severing the electrically conductive connection between the terminal and the signal terminal of the first integrated circuit using an energy pulse {column 3, line 4 – column 4, line 10}.

In re claim 2, Kuriyama shows wherein the severing step is performed by applying an electrical current pulse to the terminal of the second integrated circuit {column 3, lines 55-67}.

In re claim 3, Kuriyama shows wherein the forming step includes forming the electrically conductive connection with a portion of reduced cross sectional area as compared to the rest of the connection; and dimensioning the portion to dissipate electrostatic discharges between the terminal and the signal terminal of the first integrated circuit and to be severed during application of the energy pulse in the severing step {column 3, lines 55-67}.

In re claim 4, Kuriyama shows wherein the energy pulse used in the severing step is an electrical current pulse applied to the terminal of the second integrated circuit {column 3, lines 55-67}.

In re claim 5, Kuriyama shows disposing the first and second integrated circuits in a package having terminal pins (2/4/5) so that the signal terminal of the first integrated circuit is not accessible

form outside of the package; and connecting the terminal of the first integrated circuit and the terminal of the second integrated circuit to a respective terminal pin (5/4) of the package {column 3, lines 4-54}.

In re claim 6, Kuriyama shows wherein the severing step is performed after the step of connecting the respective terminals to the respective terminal pins {column 3, lines 4-54}.

In re claim 7, Kuriyama shows wherein the disposing step is performed so that the terminal of the second integrated circuit is not covered by the first integrated circuit {see Figure 1}.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama as applied to claims 1-7 above, and further in view of Bozso et al..

In re claim 8, Kuriyama shows in Figures 1 and 2 a method for producing an electrical connection between integrated circuits, providing a first integrated circuit (7) having a surface; disposing first and second terminal pads (11 and 12) on the surface of the first integrated circuit; forming an electrically conductive connection (10c) between the first and second terminal pads of the first integrated circuit; providing a second integrated circuit (3) having a surface; disposing first and second terminal pads (3b and 3c) on the surface of the second integrated circuit; electrically

coupling at least the first terminal pad of the second integrated circuit to a protective structure for protecting against electrostatic discharges; disposing the surfaces of the first and second integrated circuits adjacent one another; electrically joining at least one of the first and second terminal pads of the first integrated circuit to one of the first and second terminal pads of the second integrated circuit; and severing the electrically conductive connection using an energy pulse { column 3, line 4 – column 4, line 10}.

Kuriyama does not show wherein the step of disposing the surfaces includes disposing the surfaces of the first and second integrated circuits longitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit are not covered by the first integrated circuit.

Bozso et al. (herein referred to as Bozso) shows, in an analogous art related to integrated circuit packaging, in Figure 7 that two integrated circuits may be bonded together by disposing surfaces of the integrated circuits longitudinally adjacent one another so that terminal pads of one of the integrated circuits are not covered by the other integrated circuit {column 5, lines 36-39}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose the surfaces of the first and second integrated circuits longitudinally adjacent one another so that the first and second terminal pads of the second integrated circuit are not covered by the first integrated circuit as in Boss since, as evidenced by Bozso, it is well known within the packaging art to place two integrated circuits together such that their surfaces are longitudinally adjacent one another and the packaging arrangement of Bozso would provide a compact package with which to use. Furthermore, the specification contains no disclosure of either the critical nature of the claimed packaging arrangement or any unexpected results arising therefrom. Where

patentability is said to be based on a particular packaging arrangement or upon another variable recited in a claim, the applicant must show that the claimed packing arrangements are critical or yield unexpected results over the prior art.

In re claims 9 and 10, Kuriyama does not show wherein the electrically joining step is performed using an electrically conductive solderable material or a conductive adhesive material.

Bozso teaches wherein the two integrated circuits are electrically joined using an electrically conductive solderable material {column 5, lines 30-39}.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to electrically join the first and second integrated circuits of Kuriyama in view of Bozso using electrically conductive solderable material prescribed by Bozso since, as evidenced by Bozso, electrically conductive solderable material is a well known material in the art that may be used to electrically join surfaces of two integrated circuits disposed longitudinally adjacent one another and the selection of a known material on the basis of its suitability for the intended use involves only routine skill in the art. It also would have been obvious that the electrically conductive solderable material is a conductive adhesive material because solder is, as previously evidenced by Bozso, used to bond, both physically and electrically, two materials together.

In re claim 11, Kuriyama further includes electrically joining the other one of the first and second terminal pads of the first integrated circuit to the other one of the first and second terminal pads of the second integrated circuit {see Figure 1}.

Conclusion

8. Paper related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication of earlier communication from the examiner should be directed to **Kurt Eaton** at **(703) 305-0383** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via kurt.eaton@uspto.gov.

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